

WHAT IS CLAIMED IS:

1 1. A method for manufacturing integrated circuit devices including
2 capacitor structures, the method comprising:
3 providing a substrate, including an overlying thickness of first insulating
4 material;
5 forming a plurality of openings within the thickness of the first insulating
6 material and a region of the dielectric material, each of the openings including a width and a
7 height;
8 forming a barrier layer overlying an exposed surface of each of the plurality of
9 openings;
10 filling each of the openings with a metal layer, the metal layer occupying
11 substantially an entire region of each of the openings to form a plurality of metal structures,
12 each of the metal structure having a width and height;
13 planarizing a surface of the metal layer;
14 patterning the region to expose each of the metal structures to expose the
15 barrier layer overlying each of the metal structures;
16 forming an insulating layer overlying each of the exposed barrier layer
17 structures; and
18 forming a second metal layer overlying the capacitor insulating layer
19 overlying the barrier layer structures, whereupon each of the metal layer structures, overlying
20 capacitor insulating layer, and second metal layer form a capacitor structure; and
21 planarizing the second metal layer.

1 2. The method of claim 1 wherein the metal structures comprise
2 substantially copper material or tungsten or aluminum.

1 3. The method of claim 1 wherein the insulating layer is silicon nitride or
2 PECVD silicon nitride.

1 4. The method of claim 1 wherein the insulating layer is maintained at a
2 temperature below 400 degrees Celsius.

1 5. The method of claim 1 further comprising forming a dual damascene
2 interconnect structure within the first insulating material concurrently with one or more of the
3 steps of forming the integrated circuit.

6. The method of claim 1 wherein the barrier metal layer comprises
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7. The method of claim 1 wherein the second metal layer comprises tungsten filling the region occupied by the plurality of metal structures.

8. The method of claim 1 wherein the patterning comprises selective portion of the first insulating material to expose the plurality of metal structures.

9. The method of claim 8 wherein the selective removal uses an etchant C_4F_8 , CO , O_2 , CF_4N_2 , ArSF_6 , CHF_3 , CH_3F , C_4F_6 , and C_2F_6 .

10. The method of claim 1 wherein the integrated circuit is a mixed mode

11. A semiconductor integrated circuit device structure comprising:
a substrate;

a thickness of first insulating material overlying the substrate;

a capacitor region within the thickness of the first insulating material, the capacitor region extending from a lower surface of the first insulating material to an upper surface of the first insulating material, the capacitor region including a width, the width extending from the lower surface to the upper surface;

a contact region overlying the substrate within at least the capacitor region;

a lower capacitor plate formed from a plurality of vertical metal structures

10 defined within the capacitor region and connected to the contact region, each of the plurality
11 of vertical metal structures including a width and a height, each of the plurality of vertical
12 metal structures being substantially parallel to each other along a length of the height of each
13 of the vertical metal structures;

14 a barrier metal layer formed overlying exposed surfaces of each of the
15 plurality of vertical metal structures;

16 a capacitor dielectric layer overlying each of the exposed surfaces of the
17 barrier layer on each of the vertical metal structures; and

18 an upper capacitor plate formed from metal material within the capacitor
19 region overlying surfaces of the capacitor dielectric layer; and

20 a planarized surface formed from the upper capacitor plate.

1 12. The device of claim 11 wherein the metal material fills the capacitor
2 region defined in the thickness of first insulating material.

1 13. The device of claim 11 wherein the capacitor dielectric layer comprises
2 an oxide.

1 14. The device of claim 12 wherein the lower capacitor plate comprises a
2 copper material.

1 15. The device of claim 11 wherein the lower capacitor plate, the capacitor
2 dielectric, and upper capacitor plate define a metal insulator metal capacitor for a mixed
3 signal device.

1 16. The device of claim 11 further comprising an interconnect region
2 defined within the thickness of first insulating material, the interconnect region being outside
3 of the capacitor region.

1 17. A method for manufacturing integrated circuit devices including
2 capacitor structures, the method comprising:

3 providing a semiconductor substrate;

4 forming an overlying thickness of first insulating material on the
5 semiconductor substrate;

6 defining a capacitor region and an interconnect region;

7 forming a plurality of openings within the thickness of the first insulating
8 material and the capacitor region of the first insulating material, each of the openings
9 including a width and a height;

10 forming a plurality of openings within the thickness of first insulating material
11 in the interconnect region;

12 forming a barrier layer overlying an exposed surface of each of the plurality of
13 openings in the capacitor region and the interconnect region;

14 filling each of the openings with a metal material, the metal material
15 occupying substantially an entire region of each of the openings to form a plurality of metal
16 structures, each of the metal structure having a width and height;

17 planarizing a surface region of each of the metal structures;

18 patterning the capacitor region to expose the barrier layer on each of the metal
19 structures to form an opening within the capacitor region excluding the plurality of metal
20 structures and barrier layer, the plurality of metal structures and barrier layer forming a first
21 electrode structure of a capacitor;

22 forming an insulating layer overlying each of the exposed barrier layer
23 structures to form a capacitor dielectric for the capacitor;

24 filling the opening within the capacitor region using a second metal layer
25 overlying the capacitor insulating layer to form a second electrode structure of the capacitor;
26 and

27 planarizing the second metal layer.

1 18. The method of claim 17 wherein the second metal layer comprises a
2 copper material.

1 19. The method of claim 17 wherein the metal material is copper fill
2 material.